SWITCHING DEVICE HAVING A NON-LINEAR ELEMENT

CROSS REFERENCE TO RELATED APPLICATIONS

The instant application is a continuation of and claims priority to U.S. patent application Ser. No. 13/960,735, filed Aug. 6, 2013, which claims priority to and is a continuation of U.S. patent application Ser. No. 13/149,757, filed May 31, 2011, which is hereby incorporated by reference herein for all purposes.

BACKGROUND

The present invention is related to switching devices. More particularly, the present invention provides a structure and a method for forming non-volatile resistive switching memory devices characterized by a suppression of current at low bias and a high measured ON/OFF resistance ratio.

The success of semiconductor devices has been mainly driven by an intensive transistor down-scaling process. However, as field effect transistors (FET) approach sizes less than 100 nm, problems such as short channel effect start to prevent proper device operation. Moreover, such sub 100 nm device size can lead to sub-threshold slope non-scaling and increased power dissipation. It is generally believed that transistor based memories such as those commonly known as Flash memory may approach an end to scaling within a decade. Flash memory is one type of non-volatile memory device.

Other non-volatile random access memory (RAM) devices such as ferroelectric RAM (Fe RAM), magneto-resistive RAM (MRAM), organic RAM (ORAM), and phase change RAM (PCRAM), among others, have been explored as next generation memory devices. These devices often require new materials and device structures to couple with silicon based devices to form a memory cell, which lack one or more key attributes. For example, Fe-RAM and MRAM devices have fast switching characteristics and good programming endurance, but their fabrication is not CMOS compatible and size is usually large. Switching for a PCRAM device uses Joules heating, which inherently has high power consumption. Organic RAM or ORAM is incompatible with large volume silicon based fabrication and device reliability is usually poor.

As integration of memory devices increases, the size of elements is reduced while the density of elements in a given area is increased. As a result, dark current or leakage current becomes more of a problem, where leakage current can return a false result for a read operation or cause an unintentional state change in a cell. The problem of leakage current is particularly acute in two-terminal devices, in which multiple memory cells can form leakage paths through interconnecting top and bottom electrodes.

Conventional approaches to suppressing leakage current in switching devices include coupling a vertical diode to a memory element. However, the external diode approach has several disadvantages. In general, the diode fabrication process is a high temperature process, typically conducted above 500 degrees Celsius. Because most diodes rely on a P/N junction, it is difficult to scale the diode height to achieve a memory and diode structure with a desirable aspect ratio. And finally, a conventional diode is only compatible with a unipolar switching device, and not a two-way bipolar device. It is therefore desirable to have a robust and scalable method and structure for a highly integrated memory that is not adversely affected by leak currents.

BRIEF SUMMARY OF THE INVENTION

The present invention is generally related to switching devices. More particularly, the present invention provides a structure and a method for forming a non-volatile memory cell using resistive switching. It should be recognized that embodiments according the present invention have a much broader range of applicability.

In a specific embodiment, a switching device includes a substrate; a first electrode formed over the substrate; a second electrode formed over the first electrode; a switching medium disposed between the first and second electrode; and a nonlinear element disposed between the first and second electrodes and electrically coupled in series to the first electrode and the switching medium. The nonlinear element is configured to change from a first resistance state to a second resistance state on application of a voltage greater than a threshold.

The switching device includes a RRAM in an embodiment.

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The present invention has a number of advantages over conventional techniques. For example, embodiments of the present invention allow for a high density non-volatile memory characterized by high switching speed, low leakage current characteristic, and high device yield. Depending on the embodiment, one or more of these may be achieved. These and other advantages will be described below in more detail in the present specification.

BRIEF DESCRIPTION OF THE DRAWINGS

Exemplary embodiments will hereinafter be described in conjunction with the appended drawings, wherein like designations denote like elements, and wherein:

FIG. **1** illustrates a non-volatile memory device including a memory cell that has a bottom electrode, a switching medium, and a top electrode according to an embodiment of the present invention;

FIG. **2** illustrates I-V resistance switching characteristics of a resistive memory cell;

FIG. **3**A illustrates a two-terminal memory cell that is placed in an ON state by applying a program voltage $V_{PROGRAM}$ to the top electrode;

FIG. **3**B illustrates a two-terminal memory cell that is placed in an OFF state by applying an erase voltage V_{ERASE} to the top electrode;

FIG. **4** illustrates a memory array including a leakage current;

FIG. **5** illustrates a non-volatile memory cell including a nonlinear element according to an embodiment of the present invention;

FIG. **6**A illustrates I-V characteristics of a digital nonlinear element subjected to a voltage sweep;

FIG. **6**B illustrates I-V characteristics of a switch combined with a digital nonlinear element in an initially OFF state subjected to a positive voltage sweep;

FIG. **6**C illustrates I-V characteristics of a switch combined with a digital nonlinear element in an initially OFF state subjected to a negative voltage sweep;